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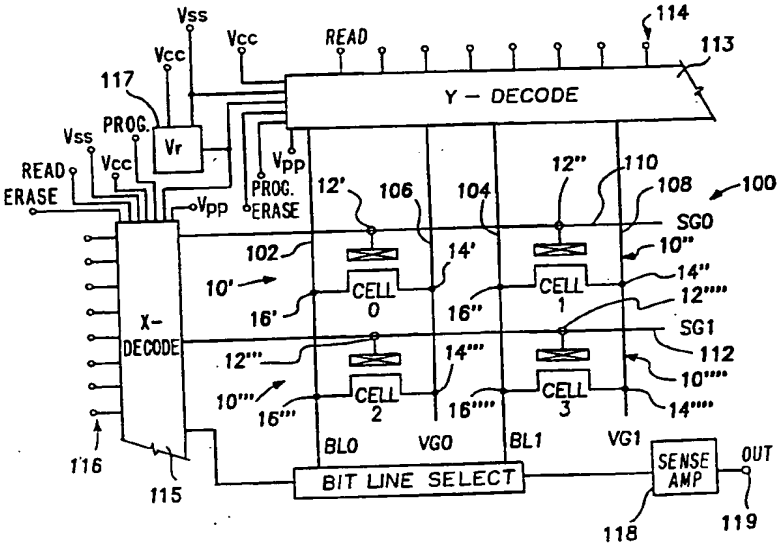

(57) Abstract

An N-channel SNOS or SONOS type memory array (100) has programmable memory states with a negative, depletion mode threshold lower in magnitude than the supply voltage V_{CC} when erased and a positive threshold when programmed. During reading, the supply voltage V_{CC} is applied to the drain (16), while a positive voltage V_R less than V_{CC}-$V_{ds,sat}$ is applied to the source (14), where $V_{ds,sat}$ is the saturation voltage of the device. A reference voltage may also be applied to the substrate (11) during a read operation. Selected devices have V_R applied to the gate (12), while inhibited devices have ground or the substrate potential V_{SS} applied to the gate (12).

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FLASH MEMORY SYSTEM, AND METHODS OF CONSTRUCTING AND UTILIZING SAME

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

This invention relates to improvements in non-volatile dielectric memory cell devices and methods for operating such devices, and more particularly to improvements in scalable non-volatile dielectric memory cell device construction and biasing circuitry used therein, and to methods for reducing disturb conditions when reading, erasing, or programming non-volatile dielectric memory cells.

2. RELEVANT BACKGROUND

Nonvolatile memory cells of the type in which a dielectric body is configured to exhibit an electric field between the channel and gate of a field effect transistor (FET) device are becoming of increased interest. In such memory cells, although various storage mechanisms may be provided by different known dielectric materials, generally, various physical or electrical changes may be selectively programmed into the cell dielectric which result in electric fields that control a current flow in the channel of the memory transistor when the cell is addressed. Usually, individual memory cells are programmed and erased by applying particular programming voltages, often much higher than normal operating read voltages, between the gate and the source, drain, and substrate of the cell transistors. Once the cell has been programmed, a current flow induced in the channel is measurably influenced by the field produced by the dielectric, sensed by various known sensing techniques, and interpreted as a logical one or zero.

One of the major problems prior art cells have experienced is a so-called "read disturb" condition. A "disturb" is condition that diminishes the quality of the data in the cell, or in some cases, actually changes the data held in the dielectric.

Disturb conditions occur primarily when a cell is read, although disturbs can occur whenever a memory array is addressed. Read disturb effects are generally only slight for each read event on any particular cell, but, in the past, read events cumulatively operate to change the information stored in the dielectric material of the cell, resulting particularly in an erased cell appearing as if it had been programmed or a programmed cell appearing as if it had been erased. A disturb condition of this proportion renders the cell, or an array in which it is embodied, virtually useless, since the number of times any cell can be read is limited.

The effects of disturb conditions are generally more widespread in a memory array than merely the particular cells being addressed. Since memory cells in most memory array constructions share some common interconnecting lines, read voltages to read a specific addressed cell are often also applied to at least some elements of adjacent and nearby cells. These unwanted voltages also may tend to create read disturb problems on the non-addressed cells, as well.

In some applications, to address these read disturb problems, multiple transistors have been employed in each memory cell to isolate the memory transistor of the cell from unintended voltages, especially when common interconnecting lines may be employed. Typically, in multiple transistor arrangements, each memory cell has three transistors, with an isolating transistor located both above and below the memory transistor. In fact, such upper isolation transistor typically may be used to select the memory cell transistor when it is addressed in order to isolate the selection voltages from the gate of the memory cell transistor itself to minimize the possibilities of read disturb events.

Although multiple transistors are widely used for voltage isolation, recently single cell nonvolatile dielectric memory arrays have been proposed. The single memory cells are addressed in read operations by an increased voltage, on the order of twice the magnitude of a supply voltage, V_{cc}, applied to the drain of the memory transistor, with V_{cc} applied to the gate and source.

This requires special voltage doubler or multiplier circuits on the memory array chip, and results in voltages applied to the transistor that are higher than necessary. Such techniques also are generally not scalable, since device sizes are being increasingly smaller but without concomitant supply voltage reductions. This produces significantly higher fields within the memory transistor and its memory retention dielectric.

SUMMARY OF THE INVENTION

In light of the above, it is, therefore, an object of the invention to provide improved non-volatile dielectric memory cell devices and methods for operating such devices.

It is another object of the invention to provide an improved non-volatile memory cell device that includes a bias circuit that enables a dielectric storage memory cell to be fully scalable, using a single transistor cell.

It is still another object of the invention to provide a method for biasing a non-volatile dielectric storage memory cell that enables a single transistor cell to be addressed without read disturb conditions to the addressed cell as well as the nonaddressed cells in the array.

It is a further object of the invention to provide a memory cell, which utilizes a non-conductive non-volatile storage element having a channel substantially fully self-aligned to a field shield isolation gate.

It is a still further object of the invention to provide a smaller cell size by utilizing field shield isolation.

Yet another object of the invention is to integrate cells into an array by utilizing a diffused bit line beneath a field shield isolation gate.

Yet another object of the invention is to reduce the write voltage and the program and erase currents.

It is yet another object of the invention to provide a novel memory cell architecture and bias scheme.

The above and further objects, details and advantages of the invention will become apparent from the following detailed description, when read in conjunction with the accompanying drawings.

The invention relates to a memory cell to construct an integrated circuit superior to known devices. More particularly, the invention comprises a memory cell that may be constructed as a single transistor non-volatile cell, integrated into a cell array. The memory cell utilizes a non-conductive non-volatile storage layer between the gate and the channel. The non-volatile storage layer may be altered by the application of an electric field or the conduction of current with its accompanying electric field between the gate and the channel regions of the transistor. Such altering of the non-volatile layer may comprise changing the stored charge in the layer, the molecular structure of the layer, or the atomic structure of the layer.

The channel is fully self-aligned to a field shield isolation gate which also permits small cell size. The non-volatile layer of material can be altered by the application of an electric field or a current with its accompanying electric field between the gate and the channel of the transistor. The non-volatile material may comprise oxides, oxynitrides, ferroelectric materials, silicon rich oxide, silicon nitride, silicon oxy-nitride, silicon rich silicon dioxide, tantalum pentoxide, carbides, ceramics, aluminum oxide, silicon carbide or ferroelectric materials, or other suitable dielectrics or multilayered dielectrics, such as SNOS, and SONOS.

Thus, according to a broad aspect of the invention, a non-volatile integrated memory circuit is presented. The circuit is formed on a semiconductor substrate, and has a memory transistor having a source, a drain, a gate, and a dielectric memory material. The dielectric memory material has programmable memory states that produce a negative transistor threshold of magnitude less than V_{cc} when the memory transistor is erased and a different threshold when the memory transistor is programmed. A biasing circuit applies selected read biasing voltages to the gate, drain, source, and substrate of the transistor. The read biasing voltages include a supply voltage, V_{cc}, applied to the drain, and a read voltage, V_r, of magnitude less than supply voltage, applied to the source and gate. A sensing circuit senses a current generated at the drain of the memory transistor in accordance

with the programmable state of the dielectric memory material. The biasing circuitry also may apply a reference voltage, V_{ss}, to the substrate during a read operation.

The dielectric memory material may be selected from the group comprising oxides, oxynitrides, ferroelectric materials, silicon rich oxide, silicon nitride, silicon oxy-nitride, silicon rich silicon dioxide, tantalum pentoxide, carbides, ceramics, aluminum oxide, silicon carbide and ferroelectric materials, or may be another suitable dielectrics or multilayered dielectrics, such as SNOS, and SONOS.

The read voltage, V_r, is selected such that it is of opposite polarity and oarger in magnitude than a threshold voltage of the memory transistor after it has been freshly erased, but less than $V_{cc} - V_{ds,sat}$, where $V_{ds,sat}$ is a saturation voltage of the memory transistor.

In accordance with another broad aspect of the invention, a non-volatile integrated memory array is presented, incorporating a plurality of memory cells that are read in a similar fashion to that next immediately above described. Additionally, the memory array may further comprise circuitry for deselecting nonaddressed memory transistors that comprises circuitry for applying selected inhibit biasing voltages to the gate, drain, and source of nonaddressed memory transistors. The inhibit biasing voltages include a supply voltage, V_{cc}, applied to the drains, and a read voltage, V_r, of magnitude less than supply voltage, applied to the sources, and a reference potential, V_{ss}, applied to the gates of the transistors of the nonaddressed cells.

In accordance to yet another broad aspect of the invention, a method is presented for operating a non-volatile integrated memory circuit having at least one memory cell with a single memory transistor formed in a semiconductor substrate and having a source, a drain, a gate, and a dielectric memory material that has programmable memory states that produce a negative transistor threshold of magnitude less than a supply voltage, V_{cc}, when the memory transistor is erased and a different threshold when the memory transistor is programmed. The method includes the step of applying read biasing voltages to the memory transistor,

including a supply voltage, V_{cc}, to the drain, and a read voltage, V_r, of magnitude less than supply voltage to the source and gate. The method includes the further step of sensing a current generated at the drain of the memory transistor in accordance a programmed state of the dielectric memory material.

The method may be applied to an array of non-volatile integrated memory cells, each cell having a single memory transistor. The method further includes the step of deselecting memory transistors of nonaddressed cells in the array by applying selected inhibit biasing voltages to the gate, drain, and source of memory transistors of the nonaddressed cells. The inhibit biasing voltages include a supply voltage, V_{cc}, applied to the drains, and a read voltage, V_r, of magnitude less than supply voltage, applied to the sources, and a reference potential, V_{ss}, applied to the gates and substrate.

The invention results in a non-volatile memory cell and array that has a smaller surface area, has lower program/erase current and power requirements, has more reliability, and has lower vulnerability to radiation than previous devices.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a schematic of a single memory cell in accordance with a preferred embodiment of the invention.

Figure 2 illustrates a schematic of an array of memory cells in accordance with another preferred embodiment of the invention.

Figure 3 illustrates a top plan view of one embodiment of the cell array shown in Figure 2.

Figure 4 illustrates a cross-sectional view taken along line 4-4 in Figure 3.

Figure 5 illustrates a cross-sectional view taken along line 5-5 in Figure 3.

Figure 6 illustrates a cross-sectional view taken along line 6-6 in Figure 3.

Figure 7 illustrates a cross-sectional view taken along line 7-7 in Figure 3.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

As seen in Figure 1, a schematic of a memory cell 10 that can be used in practicing the invention is illustrated. The

memory cell 10 is formed with a single transistor that has a storage layer of non-conducting, non-volatile material between its gate electrode 12 and the transistor channel. Additional non-conducting layers may also be provided between the gate 12 and the channel to form a multi-layer gate dielectric.

The material of the non-volatile gate dielectric is preferably of a type capable of having its properties altered by the application of an electric field or by the conduction of current with its accompanying electric field between the gate and the channel of the transistor, and imparts to the transistor negative thresholds of magnitudes less than V_{cc} by at least $V_{ds,sat}$ in a freshly erased cell. This value is typically at least 1 volt, but is greater than an amount necessary to allow a current flow in the device in a read operation. The properties that may be altered in the material are typically either a stored charge, a molecular structure change, or an atomic structure change. Such non-conducting layers may comprise insulative materials of thicknesses less than 500 angstroms.

Examples of suitable materials of which the non-volatile gate dielectric may be constructed include, but are not limited to, oxides, oxynitrides, ferroelectric materials, silicon rich oxide, silicon nitride, silicon oxy-nitride, silicon rich silicon dioxide, tantalum pentoxide, carbides, ceramics, aluminum oxide, silicon carbide or ferroelectric materials, or other suitable dielectrics or multilayered dielectrics, such as SNOS, and SONOS. These materials have such advantages over other materials that they are generally non-conductive compared to heavily doped silicon; they are capable of being semi-permanently altered on a molecular or atomic level by an electric field or current with its accompanying electric field; their retention properties affect the surface potential of the memory cell transistor; they have properties that are stable over a wide range of temperature consistent with commercial semiconductor products; and their alteration property is to the first order reversible.

The change in properties in the above-mentioned materials affects the surface potential of the channel of the transistor to significantly alter the channel conductance under bias. Thus,

different levels of conductivity correspond to different logic states. For example, an "on" or conducting state may indicate a logic '0' and an "off" or non-conducting state may indicate a logic '1'. Therefore, by sensing the drain-to-source current under bias, the state of the stored information can be determined. Since the information is stored in a non-volatile form, the information remains stored for a period of time, typically ten years or longer, regardless of whether power is applied to the memory cell 10 or any product containing the memory cell 10.

The memory cell 10 is a single transistor having a diffused source node 14, a diffused drain node 16, a gate node 12, and a substrate node 11. The non-volatile layer 18 is schematically represented as a box with a cross between the gate and the channel to denote the presence of a non-volatile film.

A preferred operation of an N-channel embodiment of a cell in accordance with the invention is summarized in Table 1 below.

Table 1

Node	Read	Read Inhibit	Erase	Program	Program Inhibit
Substrate (P-well)	V_{ss}	V_{ss}	V_{cc}	V_{pp}	V_{pp}
Source	V_r	V_r	V_{cc}	V_{pp}	V_{cc}
Drain	V_{cc}	V_{cc}	V_{cc}	V_{pp}	V_{cc}
Gate	V_r	V_{ss}	V_{pp}	V_{cc}	V_{cc}

In Table 1, V_{ss} is a reference potential, such as ground or a negative potential with respect to ground, for example V_r less than ground, V_{cc} is a supply voltage, V_{pp} is a programming voltage, and V_r is a read voltage, below described in detail. It should also be noted that the conditions shown in Table 1 are for a N-channel device within a P-well. The device could be adapted to a P-channel device by appropriately changing the bias polarities and interchanging the Erase and Program state condition. For an N-channel device, V_{ss} is a reference potential, such as ground or zero potential, V_{cc} is a positive potential with respect to V_{ss},

typically between 3.0 and 6.0 volts, V_{pp} is a negative potential with respect to V_{cc}, typically within a range of V_{ss} to -10 volts, and V_r is a positive potential with respect to V_{ss}, typically within a range of 1.0 and 3.0 volts.

The cell 10 is read by the application of a voltage difference between the drain 16 and source 14, while the gate 12 is based positive with respect to the substrate node 11 (or P-well) by an amount V_r, with the gate-to-source potential difference remaining zero. The logic state of the cell 10 may be determined by using known sensing circuitry to measure the channel current of cell 10 under the bias conditions described in the prior sentence.

One of the advantages provided by the circuit and method of the invention is that the value of V_r is less than V_{cc}. It has been found that by using gate selection on a dielectric cell by bringing the source potential up from the potential of the substrate to a value V_r. The device can be deselected by bringing the gate potential from V_{cc} to V_r, thereby turning off the source junction, and, consequently, creating no fields between the gate the substrate that may cause a disturb condition. The purpose of V_r is to allow the method or system of reading individual cells in a cell array (best seen in Figure 2 and Table 2 described hereinafter) without causing a disturb to the cells of the array, and particularly to the addressed cell(s). It should be noted that the read inhibit voltages are applied to the nonaddressed cells to actively deselect the nonaddressed cells, by applying V_r to the sources and V_{ss} to the gates of the transistors of the nonaddressed cells. Again, these voltages turn off the source junction, and, consequently, create no fields between the gate the substrate, reducing or eliminating any disturb conditions.

On the other hand, the upper limit of the magnitude of the value of V_r should be selected to be less than V_{cc}, and preferably less than $V_{cc} - V_{ds,sat}$, where $V_{ds,sat}$ is the saturation voltage of the device. Since the voltage on the drain of a cell being read is V_{cc}, the value of V_r on the source and gate should be selected to still enable sufficient current to flow to be detectable. Moreover, since the erase threshold decreases (becomes more

positive) with age, a cell containing older data produces less current when addressed. Thus, the upper limit that can be selected for V_r needs to take end of life conditions into consideration. Thus, preferably, V_r should be selected to be as close to the threshold of a freshly erased cell as possible, which allows sufficient current to flow for reliable sensing at end of life.

In contrast to the cell read operation described above, the cell 10 may be "read inhibited" by setting the gate 12 equal to the potential of the substrate 11 at V_{ss} while the drain 10 and the source 14 are set at the same potentials as used during a read operation, V_{cc} and V_r, respectively. This operation is particularly useful when the cell 10 is connected in plurality with cells that share common bit and virtual source lines. In this configuration, one cell can be read while all other cells in parallel are "read inhibited" or deselected. This operation occurs without disturbing the data stored in either the addressed and selected cells or the unaddressed and deselected cells in a read operation.

The selection of an appropriate value of V_r depends on a number of factors related to the threshold voltage of an erased device. More particularly, it is recognized that the threshold voltage of a freshly erased device is larger than that of a device at end of life. End of life is generally regarded to mean a time at which the thresholds of programmed and erased devices decay to predetermined acceptable levels, and is typically on the order of about 10 years. The range of suitable minimum values for V_r is measured with regard to a freshly erased device, and can be selected to be a value that is of opposite polarity and larger in magnitude than the maximum erase threshold. The erase threshold is used to mean the threshold voltage for reading an erased cell. It will, of course be appreciated that an erase threshold can be established by design, taking into account the choice and thickness of the gate dielectric and nonvolatile materials, the size of the memory array, the number of cells that may be contributing to the output sense current, the voltage sensing capabilities of the sensing circuitry, and so forth.

Thus, the erase threshold of a device should be such that the state of a single cell can unmistakably be sensed in the particular construction chosen, at any point during the lifetime of the stored data in that cell. So, V_r may be selected to produce a maximum predetermined cell current in a deselected freshly erased cell, which, when summed over all the deselected cells on a common bit line, each being in a freshly erased state, will produce substantially less current than is required by sensing circuitry to correctly sense a program state in a single selected cell.

The cell 10 can be erased by setting the gate 12 potential to a negative value with respect to the channel or substrate. For example, the source 14, drain 16 and P-well 11 are biased at V_{cc} while the gate is biased at V_{pp}. These conditions are held typically 10 milliseconds or less. The drain 16 or source 14, but not both simultaneously, could be allowed to "float" to the P-well potential.

In a similar manner, the cell 10 can be programmed by setting the substrate, source 14, and drain 16 to the same V_{pp} potential, while setting the gate 12 potential to a positive value with respect to the channel or source 14. For example, the source 14, drain 16 and P-well 11 are biased at V_{pp} while the gate is biased at V_{cc}. Again, the conditions are typically held for 10 milliseconds or less and the drain 16 or source 14, but not both simultaneously, could be allowed to float to the P-well potential.

Another feature of the single cell 10 device is its ability to "program inhibit" the cell 10 as shown in the Program Inhibit column of Table 1. This operation is used when a plurality of cells 10 share a common gate along a row. A single cell 10 along a row can be programmed while the other cells 10 on that row are program inhibited.

Thus, in operation, if a selected device is erased, V_r is selected such that current flows in the device when the gate and source potentials are equal to V_r and the drain potential is V_{cc}, which is larger than V_r. The potential in the erased device channel is between V_{cc} and V_r, thus preventing a "disturb"

condition by reinforcing the erase state of the dielectric. Since the device is not selected, V_{ss} is applied to the gate; consequently, no or very little current flows while the source is at V_r. If an erased device has a negative threshold voltage less than V_r in magnitude, a device with its gate at V_{ss} will be off and there will be no gate to substrate (or channel) field to disturb the non-volatile state.

On the other hand, if the device is programmed and has a positive threshold voltage, no current will flow under the read bias conditions of any of the cells. No channel will form in the programmed device and a voltage drop will occur that reinforces the programmed state, thus preventing a disturb condition. In a read inhibit condition with a programmed positive threshold voltage, a cell with its gate 12 at V_{ss}, will be off and the gate to substrate potential will be zero, which also is a non-disturb condition.

The drain 16 to source 14 current may be sensed or measured using any one of known techniques. If the cell 10 is erased, the channel is conductive and current flows from drain 16 to source 14. If cell 10 is programmed, the channel is non-conductive and none to a slight current is present.

As best seen in Figure 2, the cell 10 may be arranged in a plurality of columns and rows of identical cells (10′, 10″, 10‴, 10⁗) to form a cell array 100 to construct a high density memory product, such as a one or sixteen megabit flash memory device, or the like. The drawings illustrate a 2 x 2 array 100, but such figures are not intended to limit the number of cells 10 possible in an array 100.

As schematically shown in Figure 2, the cells 10′ and 10‴ are connected at the source nodes 14′ and 14‴ to the virtual ground line 106, designated as VGO; and the source nodes 14″ and 14⁗ of cells 10″ and 10⁗ are connected to the virtual ground line 108, designated as VG1. Likewise, the drain nodes 16′ and 16‴ of the cells 10′ and 10‴ are connected the bit line 102, designated as BL0, and the drain nodes 16″ and 16⁗ of the cells 10″ and 10⁗ are connected to bit line 104, designated as BL1.

The cells 10′ and 10′′ share a common gate line 110 (SG0), and cells 10′′′ and 10′′′′ share a common gate line 112 (SG1). Simply stated, the drain nodes 16 and source nodes 14 are "shared" among the cells 10 in columns and the gate nodes 12 are "shared" among the cells 10 in rows. Since the source nodes 14 and drain nodes 16 are not "shared" among cells 10 in any row, independent control of source lines is possible, permitting unaddressed cells to be actively deselected for elimination of high currents and "disturbed" cells.

On the other hand, cells 10 with "shared" or common drain nodes 16 and source nodes 14 have separates gate nodes 12 permitting a single addressed cell 10 to be programmed or read. Of course, an entire row of cells 10 can be read, erased or programmed, if desired.

The bit lines BL0, BL1, . . . and virtual ground lines VG0, VG1, . . . of the individual cells 10′ - 10′′′′ are addressed by signals from a Y-decoder 113, which decodes address signals applied to an input address bus 114. In like manner, the gate lines SG0, SG1, . . . are addressed by signals from an X-decoder 115, which decodes address signals applied to an input address bus 116. The X- and Y-decoders 115 and 113 each receive a read voltage Vr, from source 117, a supply voltage Vcc, a reference potential Vss, and a programming voltage Vpp, for selective application to the respective bit, virtual ground, gate lines, and substrate of the array 100, as well as read, erase, and program control signals to specify the particular function to be performed and voltage levels to be selected and applied. The construction of the voltage source V_r 117 can be a voltage divider, band gap, or other similar circuit. The control signals and addresses can be applied to the X- and Y-decoders internally or externally from the integrated circuit chip on which the array is constructed, in a manner known in the art. The current produced on the bit lines BL0, BL1, . . . is sensed by a sense amplifier 118, for delivery to an output terminal 119. The sense amplifier 118 can be of any known suitable type.

Table 2 below describes a preferred operation of the cell array 100 shown in Figure 2.

Table 2

Node	Read Cells 0 & 1 Read Inhibit Cells 2 & 3	Erase Cells 0 & 1	Program Cell 0 Program Inhibit Cell 1
Substrate (P-Well)	V_{ss}	V_{cc}	V_{pp}
SGO	V_r	V_{pp}	V_{cc}
SG1	V_{ss}	V_{cc}	V_{pp}
BLO	V_{cc}	V_{cc}	V_{pp}
VGO	V_r	Float	Float
BL1	V_{cc}	V_{cc}	V_{cc}
VG1	V_r	Float	Float

The cell array 100 can be read by sensing a current on the bit lines 102, 104 by known sensing techniques. If an erased device has a negative threshold voltage with its gate and source potential at V_r, established as described above, the erased device will be on and conducting current.

The cell array 100 enables a read system that allows a selection of individual cells 10 within a column of common cells 10 without causing a "disturb" condition. As described above, a "disturb" condition occurs when an electric field that is at a polarity that changes the state of the cell occurs between a gate and the substrate. A read inhibit bias system allows the active "deselection" of individual unaddressed cells within a column of common cells without causing a "disturb" condition. A program inhibit bias system allows the active "deselection" of individual cells within a row of common cells 10 without causing a "disturb" condition in a cell 10.

A group of cells in the array 100 can be erased by biasing a gate, such as 12' to V_{pp}, erasing all of the cells on gate line 110. Since there is no erase inhibit operation, in distinction to a program inhibit operation, all of the cells that share a common gate are erased simultaneously. By biasing one gate to V_{pp} and either connecting all other nodes to V_{cc} or allowing the other

nodes to float, only the cells with V_{pp} on the gate will be erased. The gate-to-channel potential will be zero on all other devices, thus the state in these cells will remain undisturbed. The erase bias conditions are typically established for 10 milliseconds or less.

Program conditions can be established on a common gate, and inhibited in all cells on that common gate except those for which a programmed state is desired. A program condition can be established by biasing the substrate or P-well at V_{pp} and placing a common gate at V_{cc} (such as SGO on cells 0 and 1). If an erased state is to be preserved in any of the cells on the common gate, then either or both of the source or drain nodes of that cell are biased at V_{cc} (such as in cell 1). With only one of the two at V_{cc} the other node must be allowed to float so that no current flows and the gate-to-channel voltage will be zero. During a program operation, isolation between adjacent cells can be improved with back bias by establishing a P-well 11 bias that is more negative than V_{pp}, typically by 0.5 to 2.0 volts. The program bias conditions are typically established for 10 milliseconds or less.

Since the program and program inhibit conditions are selected on a cell-by-cell basis, typical operation of a cell array will involve first erasing all the cells on a given common gate followed by a program or program inhibit operation of all of the same cells. By following this sequence, a byte, page or block of data can be stored by first erasing the data segment then programming the same segment, inhibiting where an erased state is desired. A byte is either eight or sixteen bits along a given row of cell 10, a page is a whole row of cells 10, and a block is a section of the memory array composed of several rows and columns of cells 10. In a block operation, the entire block may be erased at once followed by a sequence of page or byte program operations on the cells within the block, such that each cell is either programmed or left erased by a program inhibit. Such a sequence of operations would be called a "write", a byte write, a page write, or a block write, depending on the data size. Another possibility is to erase an entire block, but

program or inhibit within that block as data becomes available for storage at some later time, on a page or byte basis.

A topographical plan view of a typical cell array 100 that is shown schematically in Figure 2 is shown in Figure 3. The cells 10′ to 10′′′′ utilize field shield isolation means to provide isolation between nodes of adjacent cells to reduce cell size. In this embodiment, the gate conductors 110,112 may comprise doped poly-silicon layers. However, conducting materials such as aluminum, refractory metals, or other known conducting materials may be used. The bit lines 102,104 are diffused N+/N- nodes. Isolation is provided by a first poly-silicon layer field shield device 126 with a gate held at the potential of the P-well. The memory storage area is shown at 120.

As seen in Figure 4, a cross-section taken along the line 4-4 of Figure 3 illustrates a side view of the array 100. The storage dielectric 122 is shown between the substrate and poly 2 layer 110,112. The field shield 126 is formed from a poly 1 layer. The layer 110,112 and dielectric 122 are self-aligned by the use of a single mask to etch both layers as described later. The field shield 126 separates the memory channel doping areas 128.

Shown in Figure 5 is a cross-section taken along line 5-5 in Figure 3. The section shows the device between memory areas 120 and the field shield isolation means 126.

Shown in Figure 6 is a cross-section taken along line 6-6 in Figure 3 showing the device through the memory areas 120. The channel doping 128 is provided in the channel region in this figure. This doping level in the memory channel 128 is chosen to set the average of the program and erase state threshold voltages such that the value of the average of the program and erase state threshold voltages after 10 years (or end of life) is near or slightly below V_{ss}.

The implants (N+/N-) 130, 132 are best seen in Figures 6 and 7. The N- implant 132 surrounds the N+ 130 by using the same mask as that used for the N+ region 130. The N- region 132 improves the junction breakdown characteristics, improves the

endurance of the dielectric 122 and reduces the junction capacitance of the lines 102, 104, 106 and 108. The N+ region 130 provides low sheet resistance along the lines 102, 104, 106 and 108. The N+/N- (130,132) regions are constructed into the substrate before the construction of the field shield 126 so that the bit lines 102,104 and the virtual ground lines 106 and 108 can traverse beneath the poly 1 layer 126.

Figure 7 illustrates a cross section taken along line 7-7 in Figure 3 which shows the array 100 cut between memory areas 120. Note that the N+/N- (130,132) forming bit lines 102,104 and virtual ground lines 106 and 108 continue between cells beneath field shield 126.

The cell described above can be constructed using many different processing techniques. One process flow is described here in outline form using a SONOS cell construction. The dielectric is a stack of tunnel oxide grown on the substrate, silicon oxy-nitride deposited on the tunnel oxide, and a deposited layer of silicon dioxide. An N-type starting wafer is assumed. Ranges are supplied for some thicknesses, times and temperatures. These ranges are provided for clarification of function, and not meant to indicate the only acceptable values. Only the processing steps that are required to construct the memory cell are included. Other processing steps that are required for integration with other circuit elements and interconnection can be performed in addition to the steps listed below by using techniques that are commonly known by those skilled in the art of integrated circuit processing.

1. P-Well Construction
   Oxidation (100-200 Angstroms)
   P-Well Photomasking Steps
   P-Well Boron Implant
   Photoresist Removal
   P-Well Drive (1000-1200 degrees C, 2 to 12 hours)

2. Bit-line Formation
   Clean (Etch to remove 100-200 Angstroms SiO_2)
   Oxidation (100-200 Angstroms)
   Silicon Nitride Deposition (1000-2000 Angstroms)
   Bit-Line Photomasking Steps
   Silicon Nitride Etch (Reactive Plasma Etching)

N- Implant (Phosphorous 1E14-5E15/cm^2)
N+ Implant (Arsenic 1E15-1E16/cm^2)
Photoresist Removal
Oxidation (500-2000 Angstroms)
Silicon Nitride Removal (Hot Phosphoric Acid)

3. Field Shield
Clean (Etch to remove 100-200 Angstroms)
Threshold Adjust Implant (Boron 1E11-1E12/cm^2)
Gate Oxidation (100-500 Angstroms)
Poly 1 Deposition (2000-5000 Angstroms)
Poly Doping ($POCl_3$, 900 Degrees C)
Etch (To Bare Poly)
Poly 1 Photomasking Steps
Poly 1 Etch (Reactive Plasma Etch)
Photoresist Removal

4. Spacer Oxide Formation
Deposit Conformal CVD Oxide (1000-4000 Angstroms)
Anisotropic Oxide Etch (Reactive Plasma Etch to Substrate)
Clean
Oxidation (100-500 Angstroms)

5. SONOS Cell Construction
Threshold Implant (Boron or phosphorus 1E11-1E12/cm^2)
Clean (Etch 100-500 Angstroms, Bare Silicon in Cell Channel)
Tunnel Oxide (0-25 Angstroms)
Silicon Oxy-Nitride Deposition (10-300 Angstroms)
Top Oxide Deposition (0-100 Angstroms)
Poly 2 Depositions (2000-5000 Angstroms)
Poly 2 Doping (Phosphorus, Ion Implant 1E15-5E16/cm^2)
Implant Anneal (800-900 Degrees C)
Poly 2 Photomasking Steps
SONOS Etch (Reactive Plasma Etch)
Photoresist Removal

We claim:

1. A non-volatile integrated memory circuit, comprising:

a semiconductor substrate;

a memory transistor formed in said substrate, said memory transistor having a source, a drain, a gate, and a dielectric memory material that has programmable memory states that produce a negative transistor threshold of magnitude less than V_{cc} when the memory transistor is erased and a different threshold when the memory transistor is programmed;

biasing circuitry for applying selected read biasing voltages to the gate, drain, and source of said transistor, said read biasing voltages including a supply voltage, V_{cc}, applied to the drain, and a read voltage, V_r, of magnitude less than supply voltage, applied to the source and gate;

and sensing circuitry for sensing a current generated at the drain of said memory transistor in accordance with the programmable state of said dielectric memory material.

2. The non-volatile integrated memory circuit of claim 1 wherein said biasing circuitry further comprises circuitry for applying a voltage to the substrate.

3. The non-volatile integrated memory circuit of claim 2 wherein said voltage applied to the substrate is a reference potential, V_{ss}.

4. The non-volatile integrated memory circuit of claim 3 wherein said reference potential is ground.

5. The non-volatile integrated memory circuit of claim 3 wherein said reference potential is V_r less than ground.

6. The non-volatile integrated memory circuit of claim 1 wherein said dielectric memory material is selected from the group comprising oxides, oxynitrides, ferroelectric materials, silicon rich oxide, silicon nitride, silicon oxy-nitride, silicon rich

silicon dioxide, tantalum pentoxide, carbides, ceramics, aluminum oxide, silicon carbide and ferroelectric materials.

7. The non-volatile integrated memory circuit of claim 1 wherein said dielectric memory material is a multilayered dielectric.

8. The non-volatile integrated memory circuit of claim 7 wherein said multilayered dielectric is SNOS.

9. The non-volatile integrated memory circuit of claim 7 wherein said multilayered dielectric is SONOS.

10. The non-volatile integrated memory circuit of claim 1 wherein said read voltage is of magnitude larger than a threshold voltage of the memory transistor after it has been freshly erased.

11. The non-volatile integrated memory circuit of claim 1 wherein said read voltage is less than $V_{cc} - V_{ds,sat}$, where $V_{ds,sat}$ is a saturation voltage of the memory transistor.

12. A non-volatile integrated memory array, comprising:

a semiconductor substrate;

a plurality of addressable memory transistors in said substrate, each of said memory transistors having a source, a drain, a gate, and a dielectric memory material that has programmable memory states that produce a negative transistor threshold of magnitude less than V_{cc} when the memory transistor is erased and a different threshold when the memory transistor is programmed;

biasing circuitry for applying selected read biasing voltages to the gate, drain, and source of at least an addressed one of said memory transistor, said read biasing voltages including a supply voltage, V_{cc}, applied to the drain, and a read voltage, V_r, of magnitude less than supply voltage, applied to the source and gate;

and sensing circuitry for sensing a current generated at the drain of said memory transistor in accordance with the programmable state of said dielectric memory material of said addressed memory transistor.

13. The non-volatile integrated memory array of claim 12 further comprising circuitry for deselecting nonaddressed memory transistors.

14. The non-volatile integrated memory circuit of claim 13 wherein said biasing circuitry further comprises circuitry for applying a voltage to the substrate.

15. The non-volatile integrated memory circuit of claim 14 wherein said voltage applied to the substrate is a reference potential, V_{ss}.

16. The non-volatile integrated memory circuit of claim 14 wherein said voltage applied to the substrate is a V_r less than ground.

17. The non-volatile integrated memory circuit of claim 15 wherein said reference potential is ground.

18. The non-volatile integrated memory array of claim 14 wherein said circuitry for deselecting nonaddressed memory transistors comprises circuitry for applying selected inhibit biasing voltages to the gate, drain, and source of nonaddressed memory transistors, said inhibit biasing voltages including a supply voltage, V_{cc}, applied to the drains, and a read voltage, V_r, of magnitude less than supply voltage, applied to the sources, and a reference potential, V_{ss}, applied to the gates and the substrate.

19. The non-volatile integrated memory circuit of claim 12 wherein said dielectric memory material is selected from the group comprising oxides, oxynitrides, ferroelectric materials, silicon rich oxide, silicon nitride, silicon oxy-nitride, silicon

rich silicon dioxide, tantalum pentoxide, carbides, ceramics, aluminum oxide, silicon carbide and ferroelectric materials.

20. The non-volatile integrated memory circuit of claim 12 wherein said dielectric memory material is a multilayered dielectric.

21. The non-volatile integrated memory circuit of claim 20 wherein said multilayered dielectric is SNOS.

22. The non-volatile integrated memory circuit of claim 20 wherein said multilayered dielectric is SONOS.

23. The non-volatile integrated memory circuit of claim 12 wherein said read voltage is of magnitude larger than a threshold voltage of the memory transistor after it has been freshly erased.

24. The non-volatile integrated memory circuit of claim 12 wherein said read voltage is less than $V_{cc} - V_{ds,sat}$, where $V_{ds,sat}$ is a saturation voltage of the memory transistor.

25. A method for operating a non-volatile integrated memory circuit having at least one memory cell with a single memory transistor having a source, a drain, a gate, and a dielectric memory material that has programmable memory states that produce a negative transistor threshold of magnitude less than a supply voltage, V_{cc}, when the memory transistor is erased and a different threshold when the memory transistor is programmed, comprising:

applying read biasing voltages to said memory transistor, including a supply voltage, V_{cc}, to the drain, and a read voltage, V_r, of magnitude less than supply voltage to the source and gate;

and sensing a current generated at the drain of said memory transistor in accordance a programmed state of said dielectric memory material.

26. The method of claim 25 further comprising applying a further read biasing voltage by applying a voltage to the substrate.

27. The method of claim 26 wherein said step of applying a voltage to the substrate comprises applying a reference potential, V_{ss} to said substrate.

28. The method of claim 25 further comprising selecting said dielectric material from the group comprising oxides, oxynitrides, ferroelectric materials, silicon rich oxide, silicon nitride, silicon oxy-nitride, silicon rich silicon dioxide, tantalum pentoxide, carbides, ceramics, aluminum oxide, silicon carbide and ferroelectric materials.

29. The method of claim 25 further comprising forming said dielectric memory material from a multilayered dielectric.

30. The method of claim 25 further comprising forming said dielectric memory material from SNOS.

31. The method of claim 25 further comprising forming said dielectric memory material from SONOS.

32. The method of claim 25 further comprising establishing said read voltage to have a magnitude larger than a threshold voltage of the memory transistor after it has been freshly erased.

33. The method of claim 25 further comprising establishing said read voltage to have a magnitude less than $V_{cc} - V_{ds,sat}$, where $V_{ds,sat}$ is a saturation voltage of the memory transistor.

34. A method for reading an array of non-volatile integrated memory cells, each cell having a single memory transistor having a source, a drain, a gate, and a dielectric memory material that has programmable memory states that produce a negative transistor threshold of magnitude less than a supply voltage, V_{cc}, when the

memory transistor is erased and a different threshold when the memory transistor is programmed, comprising:

applying read biasing voltages to a memory transistor of an addressed one of said cells, said read biasing voltages including a supply voltage, V_{cc}, to the drain, and a read voltage, V_r, of magnitude less than supply voltage to the source and gate;

and sensing a current generated at the drain of said memory transistor in accordance a programmed state of said dielectric memory material.

35. The method of claim 34 further comprising deselecting memory transistors of nonaddressed cells.

36. The method of claim 35 wherein said step of deselecting memory transistors of nonaddressed cells comprises applying selected inhibit biasing voltages to the gate, drain, and source of memory transistors of said nonaddressed cells, said inhibit biasing voltages including a supply voltage, V_{cc}, applied to the drains, and a read voltage, V_r, of magnitude less than supply voltage, applied to the sources, and a reference potential, V_{ss}, applied to the gates.

37. The method of claim 34 further comprising applying a read biasing voltage to the substrate.

38. The method of claim 37 wherein said step of applying a read biasing voltage to the substrate comprises applying a reference potential, V_{ss}, to said substrate.

39. The method of claim 37 wherein said step of applying a read biasing voltage to the substrate comprises applying a reference potential of Vr less than ground to said substrate.

40. The method of claim 34 further comprising selecting said dielectric memory material is from the group comprising oxides, oxynitrides, ferroelectric materials, silicon rich oxide, silicon nitride, silicon oxy-nitride, silicon rich silicon dioxide,

tantalum pentoxide, carbides, ceramics, aluminum oxide, silicon carbide and ferroelectric materials.

41. The method of claim 34 further comprising selecting said dielectric memory material is a multilayered dielectric.

42. The method of claim 41 wherein said step of selecting said dielectric memory material is a multilayered dielectric is selecting SNOS.

43. The method of claim 41 wherein said step of selecting said dielectric memory material is a multilayered dielectric is selecting SONOS.

44. The method of claim 34 further comprising establishing said read voltage to have a magnitude larger than a threshold voltage of the memory transistor after it has been freshly erased.

45. The method of claim 34 further establishing said read voltage to have a magnitude less than $V_{cc} - V_{ds,sat}$, where $V_{ds,sat}$ is a saturation voltage of the memory transistor.

AMENDED CLAIMS

[received by the International Bureau on 22 March 1994 (22.03.94), original claims 1,3,10-12,15,16,18,23-25,27,32-34,36,38,40,44 and 45 amended; other claims unchanged (8 pages)]

1. A non-volatile integrated memory circuit, comprising:

a semiconductor substrate;

a memory transistor formed in said substrate, said memory transistor having a source, a drain, a gate, and a dielectric memory material that has programmable memory states that produce a first transistor threshold of magnitude less than a magnitude of a supply voltage, V_{cc}, when the memory transistor is erased and a different threshold when the memory transistor is programmed;

biasing circuitry for applying selected read biasing voltages to the gate, drain, and source of said transistor, said read biasing voltages including a read voltage, V_r, of magnitude less than the magnitude of the supply voltage applied to the source and gate, with the supply voltage applied between the drain the the substrate;

and sensing circuitry for sensing a current generated at the drain of said memory transistor in accordance with the programmable state of said dielectric memory material.

2. The non-volatile integrated memory circuit of claim 1 wherein said biasing circuitry further comprises circuitry for applying a voltage to the substrate.

3. The non-volatile integrated memory circuit of claim 2 wherein said memory transistor is an n-channel memory transistor, said supply voltage has a magnitude, V_{cc}, applied to the drain, and said voltage applied to the substrate is a reference potential, V_{ss}.

4. The non-volatile integrated memory circuit of claim 3 wherein said reference potential is ground.

5. The non-volatile integrated memory circuit of claim 3 wherein said reference potential is V_r less than ground.

6. The non-volatile integrated memory circuit of claim 1 wherein said dielectric memory material is selected from the group comprising oxides, oxynitrides, ferroelectric materials, silicon rich oxide, silicon nitride, silicon oxy-nitride, silicon rich silicon dioxide, tantalum pentoxide, carbides, ceramics, aluminum oxide, silicon carbide and ferroelectric materials.

7. The non-volatile integrated memory circuit of claim 1 wherein said dielectric memory material is a multilayered dielectric.

8. The non-volatile integrated memory circuit of claim 7 wherein said multilayered dielectric is SNOS.

9. The non-volatile integrated memory circuit of claim 7 wherein said multilayered dielectric is SONOS.

10. The non-volatile integrated memory circuit of claim 1 wherein said memory transistor is an n-channel device, said supply voltage is applied to the drain, and said read voltage is of magnitude larger than a threshold voltage of the memory transistor after it has been freshly erased.

11. The non-volatile integrated memory circuit of claim 1 wherein a difference between a potential on the drain of said memory transistor and said read voltage is of magnitude greater than $V_{cc} - V_{ds,sat}$, where $V_{ds,sat}$ is the magnitude of the saturation voltage of the memory transistor.

12. A non-volatile integrated memory array, comprising:

a semiconductor substrate;

a plurality of addressable memory transistors in said substrate, each of said memory transistors having a source, a drain, a gate, and a dielectric memory material that has programmable memory states that produce a first threshold of magnitude less than a magnitude of a supply voltage when the memory transistor is erased and a different threshold when the memory transistor is programmed;

biasing circuitry for applying selected read biasing voltages to the gate, drain, and source of at least an addressed one of said memory transistors, said read biasing voltages including a read voltage, V_r, of magnitude less than the supply voltage, applied to the source and gate, with the supply voltage applied between the drain and substrate;

and sensing circuitry for sensing a current generated at the drain of said memory transistor in accordance with the programmable state of said dielectric memory material of said addressed memory transistor.

13. The non-volatile integrated memory array of claim 12 further comprising circuitry for deselecting nonaddressed memory transistors.

14. The non-volatile integrated memory circuit of claim 13 wherein said biasing circuitry further comprises circuitry for applying a voltage to the substrate.

15. The non-volatile integrated memory circuit of claim 14 wherein said memory transistors are an n-channel memory transistors, said supply voltage is applied to the drains of the n-channel memory transistors, and said voltage applied to the substrate is a reference potential, V_{ss}.

16. The non-volatile integrated memory circuit of claim 15 wherein said reference potential is V_r less than ground.

17. The non-volatile integrated memory circuit of claim 15 wherein said reference potential is ground.

18. The non-volatile integrated memory array of claim 13 wherein said nonaddressed memory transistors are n-channel devices and said circuitry for deselecting nonaddressed memory transistors comprises circuitry for applying selected inhibit biasing voltages to the gate, drain, and source of nonaddressed memory transistors, said inhibit biasing voltages including a supply

voltage applied to the drains, and a read voltage, V_r, of magnitude less than the supply voltage applied to the sources, and a reference potential, V_{ss}, applied to the gates.

19. The non-volatile integrated memory circuit of claim 12 wherein said dielectric memory material is selected from the group comprising oxides, oxynitrides, ferroelectric materials, silicon rich oxide, silicon nitride, silicon oxy-nitride, silicon rich silicon dioxide, tantalum pentoxide, carbides, ceramics, aluminum oxide, silicon carbide and ferroelectric materials.

20. The non-volatile integrated memory circuit of claim 12 wherein said dielectric memory material is a multilayered dielectric.

21. The non-volatile integrated memory circuit of claim 20 wherein said multilayered dielectric is SNOS.

22. The non-volatile integrated memory circuit of claim 20 wherein said multilayered dielectric is SONOS.

23. The non-volatile integrated memory circuit of claim 12 wherein said memory transistors are n-channel devices and said read voltage is of magnitude larger than a threshold voltage of the memory transistor after it has been freshly erased.

24. The non-volatile integrated memory circuit of claim 12 wherein the potential difference between said voltage applied to the drain and said read voltage is of magnitude greater than the supply voltage minus $V_{ds,sat}$, where $V_{ds,sat}$ is the magnitude of the saturation voltage of the memory transistor.

25. A method for operating a non-volatile integrated memory circuit having at least one memory cell with a single memory transistor having a source, a drain, a gate, and a dielectric memory material that has programmable memory states that produce a first transistor threshold of magnitude less than a magnitude

of a supply voltage, when the memory transistor is erased and a different threshold when the memory transistor is programmed, comprising:

applying read biasing voltages to said memory transistor, including a read voltage, V_r, of magnitude less than the magnitude of the supply voltage to the source and gate, with the supply voltage applied between the drain and substrate;

and sensing a current generated at the drain of said memory transistor in accordance with a programmable state of dielectric memory material.

26. The method of claim 25 further comprising applying a further read biasing voltage by applying a voltage to the substrate.

27. The method of claim 26 wherein said memory transistor is an n-channel device and said step of applying read biasing voltages comprises applying said voltage to the substrate at a reference potential, V_{ss}, and applying said supply voltage to the drain.

28. The method of claim 25 further comprising selecting said dielectric material from the group comprising oxides, oxynitrides, ferroelectric materials, silicon rich oxide, silicon nitride, silicon oxy-nitride, silicon rich silicon dioxide, tantalum pentoxide, carbides, ceramics, aluminum oxide, silicon carbide and ferroelectric materials.

29. The method of claim 25 further comprising forming said dielectric memory material from a multilayered dielectric.

30. The method of claim 25 further comprising forming said dielectric memory material from SNOS.

31. The method of claim 25 further comprising forming said dielectric memory material from SONOS.

32. The method of claim 25 wherein said memory transistor is an n-channel device and said applying read biasing voltages further

comprises establishing said read voltage to have a magnitude larger than a threshold voltage of the memory transistor after it has been freshly erased, and applying said supply voltage applied to the drain of said n-channel device.

33. The method of claim 25 wherein said biasing further comprises establishing the potential difference between the drain voltage and said read voltage to have a magnitude larger than the supply voltage minus $V_{ds,sat}$, where $V_{ds,sat}$ is the magnitude of a saturation voltage of the memory transistor.

34. A method for reading an array of non-volatile integrated memory cells, each cell having a single memory transistor having a source, a drain, a gate, and a dielectric memory material that has programmable memory states that produce a first transistor threshold of magnitude less than a supply voltage when the memory transistor is erased and a different threshold when the memory transistor is programmed, comprising:

applying read biasing voltages to a memory transistor of an addressed one of said cells, said read biasing voltages including a read voltage, V_r, of magnitude less than the magnitude of the supply voltage to the source and gate and with the supply voltage applied between the drain and substrate;

and sensing a current generated at the drain of said memory transistor in accordance with a programmable state of said dielectric memory material.

35. The method of claim 34 further comprising deselecting memory transistors of nonaddressed cells.

36. The method of claim 35 wherein said deselected memory transistor is an n-channel device and said step of deselecting memory transistors of nonaddressed cells comprises applying selected inhibit biasing voltages to the gate, drain, and source of memory transistors of said nonaddressed cells, said inhibit biasing voltages including the supply voltage, V_{cc}, applied to the drains, and a read voltage, V_r, of magnitude less than the

supply voltage, applied to the sources, and a reference potential, V_{ss}, applied to the gates.

37. The method of claim 34 further comprising applying a read biasing voltage to the substrate.

38. The method of claim 37 wherein said memory transistors are n-channel devices and said step of applying a read biasing voltage to the substrate comprises applying a reference potential, V_{ss}, to said substrate, and establishing said voltage applied to the drain at the supply voltage, V_{cc}.

39. The method of claim 37 wherein said step of applying a read biasing voltage to the substrate comprises applying a reference potential of V_r less than ground to said substrate.

40. The method of claim 34 further comprising selecting said dielectric memory material from the group comprising oxides, oxynitrides, ferroelectric materials, silicon rich oxide, silicon nitride, silicon oxy-nitride, silicon rich silicon dioxide, tantalum pentoxide, carbides, ceramics, aluminum oxide, silicon carbide and ferroelectric materials.

41. The method of claim 34 further comprising selecting said dielectric memory material is a multilayered dielectric.

42. The method of claim 41 wherein said step of selecting said dielectric memory material is a multilayered dielectric is selecting SNOS.

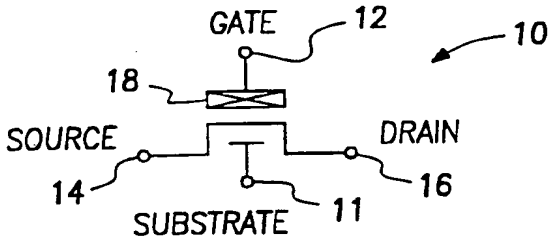
43. The method of claim 41 wherein said step of selecting said dielectric memory material is a multilayered dielectric is selecting SONOS.

44. The method of claim 34 wherein said memory transistors are n-channel devices and said biasing further comprises establishing said read voltage to have a magnitude larger than a threshold

voltage of the memory transistor after it has been freshly erased, and said voltage applied to the drain at the supply voltage, V_{cc}.

45. The method of claim 34 further establishing the potential difference between said voltage applied to the drain and said read voltage to have a magnitude greater than the supply voltage minus $V_{ds,sat}$, where $V_{ds,sat}$ is the magnitude of a saturation voltage of the memory transistor.

FIG. 1


GATE
12
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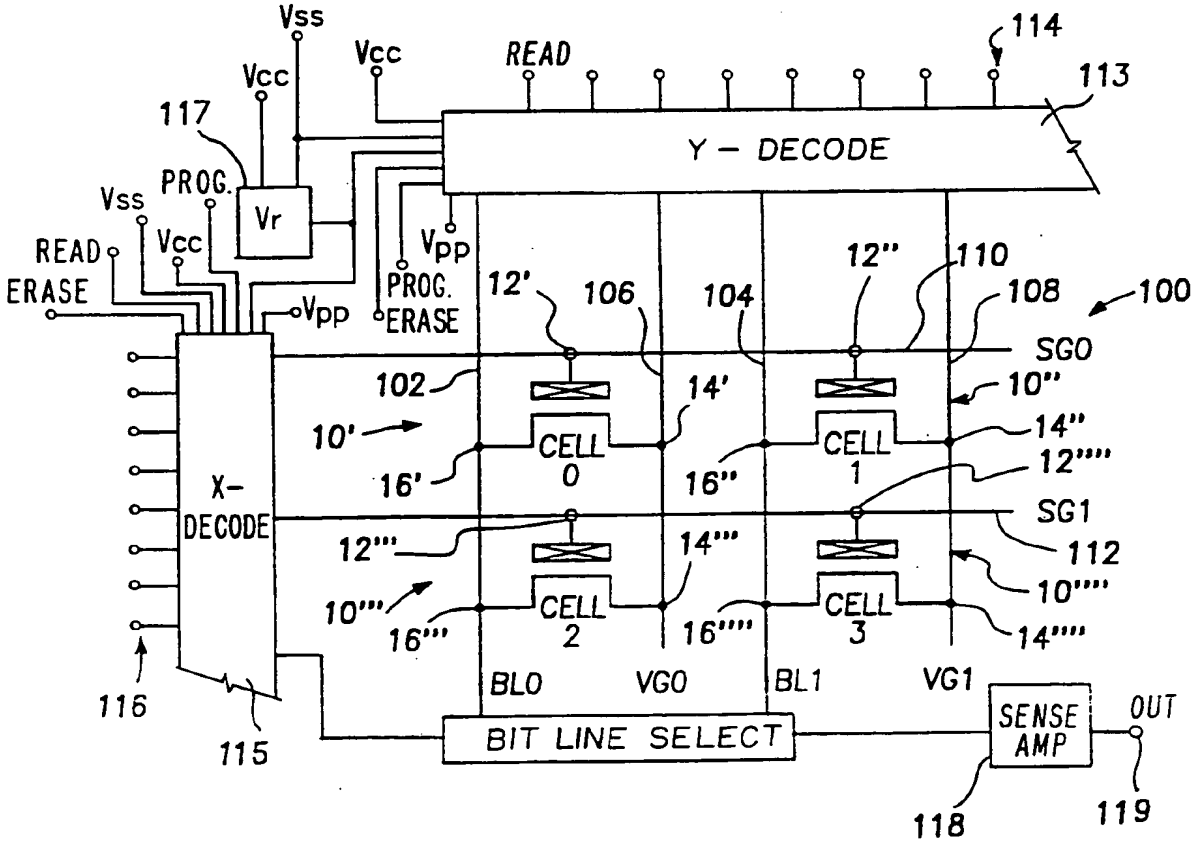
SOURCE
DRAIN
14
16
SUBSTRATE
11

FIG. 2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Vcc
Vcc
READ
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113
117
Y – DECODE
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Vr
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READ
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Vpp
PROG.
ERASE
Vpp
12'
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SG0
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14'
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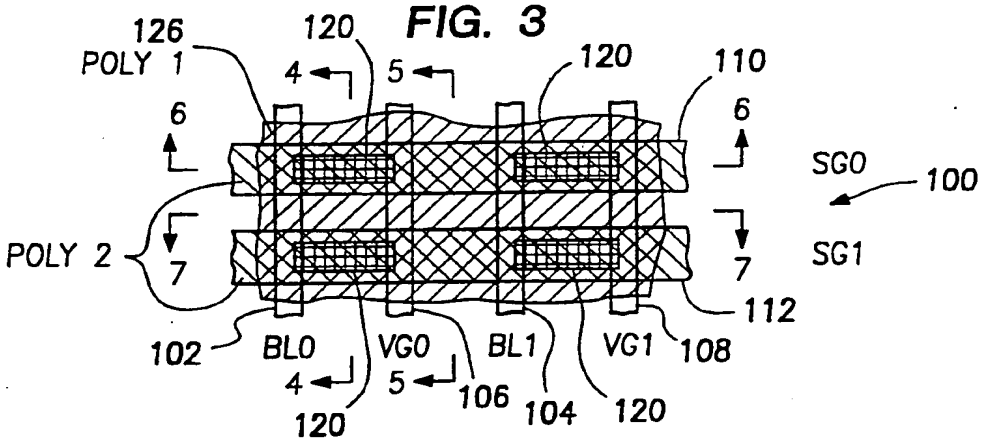
VG1
SENSE AMP
OUT
115
BIT LINE SELECT
118
119

FIG. 3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POLY 1
120
4
5
120
110
6
6
SG0
100
POLY 2
7
7
SG1
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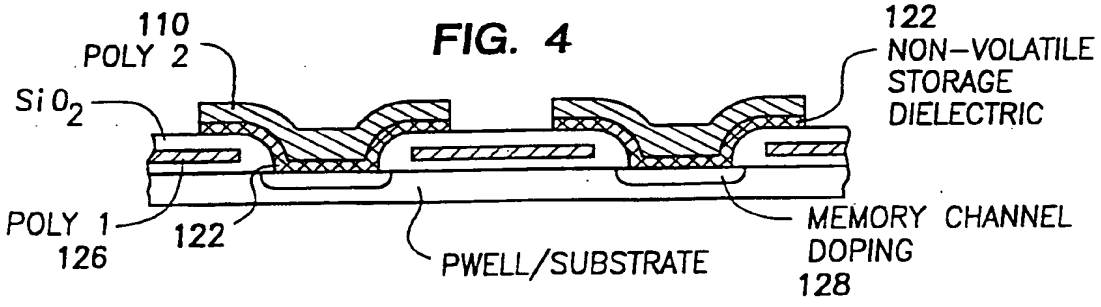
102
BL0
VG0
BL1
VG1
108
4
5
106
104
120
120

FIG. 4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SiO2
122
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DIELECTRIC
POLY 1
126
122
PWELL/SUBSTRATE
MEMORY CHANNEL
DOPING
128

FIG. 5

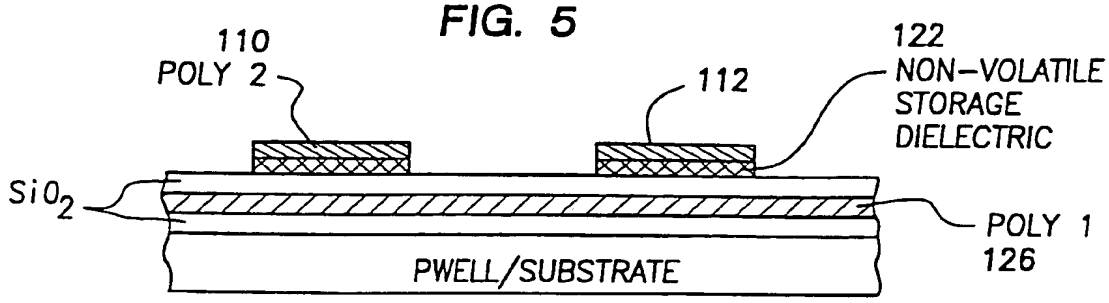


FIG. 6

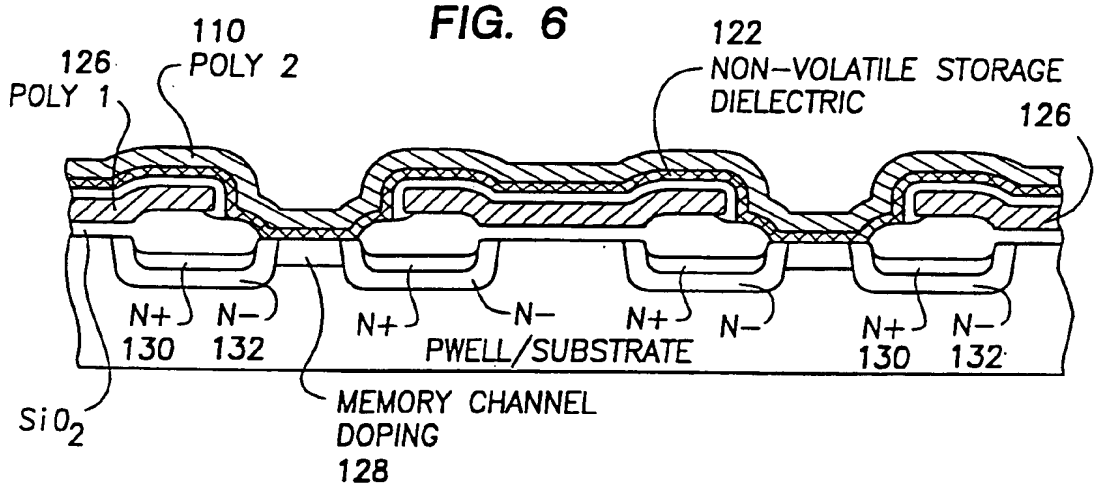
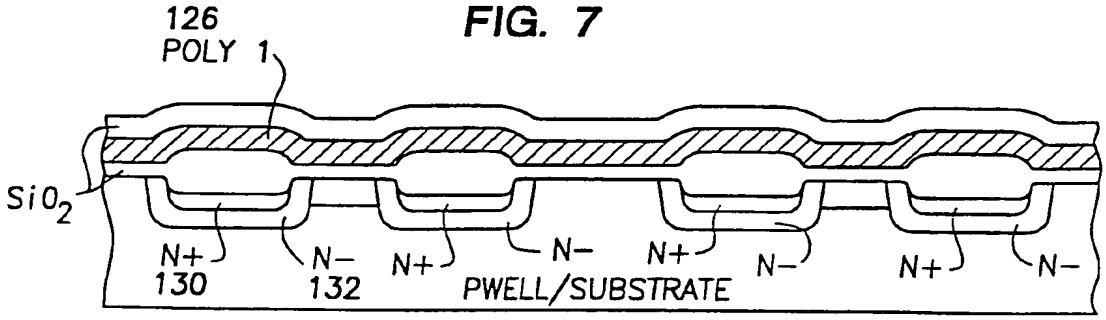


FIG. 7



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/10485

A. CLASSIFICATION OF SUBJECT MATTER
IPC(5) :G11C 11/40
US CL :365/184
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 365/184, 186; 257/324

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 4,769,787 (Furusawa et al) 06 September 1988, See the whole document	1-45
A	US, A, 4,264,376 (Yatsuda et al) 28 April 1981, See the whole document	6-8, 19-21, 40-42
A	US, A, 4,306,353 (Jacobs et al) 22 December 1981, See the whole document	6-9, 19-22, 40-43

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 26 January 1994	Date of mailing of the international search report 04 FEB 1994
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. NOT APPLICABLE	Authorized officer For WILLIAM D. LARKINS Telephone No. (703) 308-4941

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